**UNITRODE**

**UCC2750**
**UCC3750**

**PRELIMINARY**

# Source Ringer Controller

## FEATURES

- Provides Control for Flyback Based Four Quadrant Amplifier Topology
- Onboard Sine Wave Reference with Low THD
- Selectable Ringing Frequency for Different Phone Systems (20Hz, 25Hz and 50Hz)
- Programmable Output Amplitude and DC Offset
- AC Current Limiting Supports Off Hook Detection
- DC Current Limiting for Short Circuit Protection
- Secondary Side Voltage Mode Control
- Operates from a Single 5V Supply

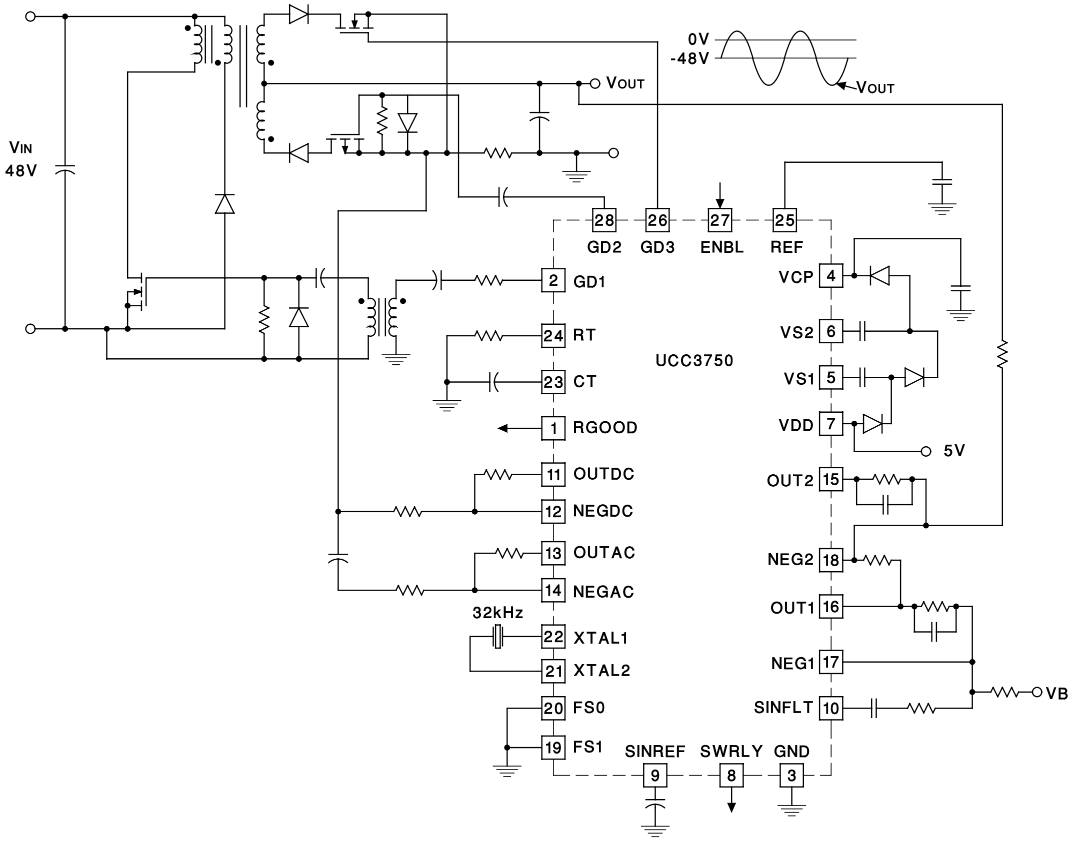
## DESCRIPTION

The UCC3750 Source Ringer Controller provides a complete control and drive solution for a four quadrant flyback-based ring generator circuit. The IC controls a primary side switch, which is modulated when power transfer is taking place from input to output. It also controls two secondary switches which act as synchronous rectifier switches during positive power flow. These switches are pulse-width-modulated when the power is being delivered back to the source.

The UCC3750 has an onboard sine wave reference with programmable frequencies of 20Hz, 25Hz and 50Hz. The reference is derived from a high-frequency (32kHz) crystal connected externally. Two frequency-select pins control an internal divider to give a sinusoidal output at 20Hz, 25Hz or 50Hz. The ring generator can also be used at other frequencies by supplying externally generated sine-waves to the chip or by clocking the crystal input at a fixed multiple of the desired frequency.

Other features included in the UCC3750 are programmable AC and DC current limits (with buffer amplifiers), a charge-pump circuit for gate drive voltage, internal 3V and 7.5V references, a triangular clock oscillator and a buffer amplifier for adding programmable DC offset to the output voltage.

## TYPICAL APPLICATION



UDG-96171-1

7/97

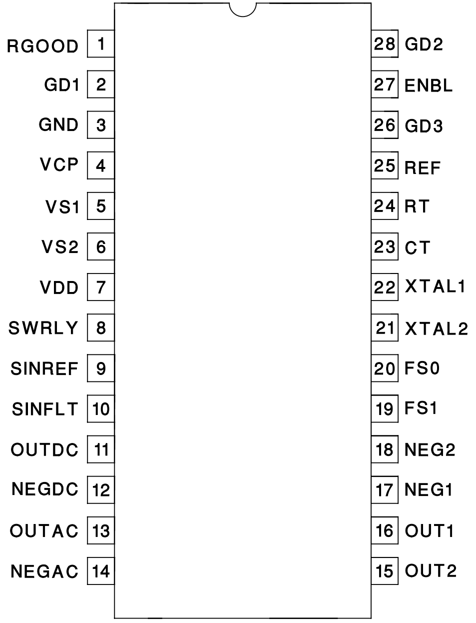
## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Input Supply Voltage | |
| VDD | 7.5V |
| Maximum Forced Voltage | |
| VCP | –0.3V to 13.2V |
| VS1, VS2 | –0.3V to 5V |
| OUT1, OUT2, OUTAC, OUTDC | |
| Maximum Forced Voltage | –0.3V to 7.5V |
| Maximum Forced Current | Internally Limited |
| NEG1, NEG2, NEGAC, NEGDC | |
| Maximum Forced Voltage | –0.3V to 7.5V |
| SINREF, SINFLT | |
| Maximum Forced Voltage | –0.3V to 7.5V |
| Logic Inputs | |
| Maximum Forced Voltage | –0.3V to 7.5V |
| Reference Output Current (REF) | Internally Limited |
| Output Current (GD1, GD2, GD3) | |
| Pulsed | 1.5A |
| Storage Temperature | –65°C to +150°C |
| Junction Temperature | –55°C to +150°C |
| Lead Temperature (Soldering, 10 Sec.) | +300°C |

*Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of the specified terminal. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500ns. Consult Packaging Section of Databook for thermal limitations and considerations of packages.*

## CONNECTION DIAGRAM

**DIL-28, SOIC- 28 (Top View)**
**N Package, DW Package**



**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for $T_A$ = 0°C to 70°C for the UCC3750, –40°C to +85°C for the UCC2750, RT = 14k, CT = 470pF, $C_{REF}$ = 0.1µF, FS0 = 0, FS1 = 0, VDD = 5V. $T_A$ = $T_J$.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **VDD Supply** | | | | | |
| Supply Current - Active | With 12V Supplied to $V_{CP}$ and Charge Pump Disabled | | 0.5 | | mA |
| **Internal Reference w/External Bypass** | | | | | |
| Output Voltage (REF) | | 7.3 | 7.55 | 7.8 | V |
| Load Regulation | $I_{REF}$ = 0mA – 2mA | | 60 | | mV |
| Line Regulation | VCP = 10V to 13V, $I_{REF}$ = 1mA | | 3 | | mV |
| **Amplifier** | | | | | |
| Input Voltage | Error, DC Offset and AC Limit Amplifiers | | 3 | | V |
| | DC Limit Amplifier | | 0.75 | | V |
| Input Bias Current | | | 500 | | nA |
| AVOL | $V_{IN}$ = 2V to 4V | | 80 | | dB |
| | DC Limit Amplifier, $V_{IN}$ = 0V to 1.5V | | 80 | | dB |
| VOH | Source 1mA | | 5 | | V |
| VOL | Sink 1mA | | 0.2 | | V |
| Gain Bandwidth Product | (See Frequency Response Curve, Figure 10) | | 3 | | MHz |
| Short Circuit Current | $V_{IN}$ = 0V and 5V with $V_{OUT}$ = 0V and 5V | | 2 | | mA |
| **Sine Reference** | | | | | |
| Accuracy | $T_J$ = 25°C, Program Frequency - Reference Frequency | –1 | 0 | 1 | Hz |
| Total Harmonic Distortion | (Note 1) | | | 2 | % |
| Amplitude | Peak | 0.475 | 0.5 | 0.525 | V |
| Offset | | 2.85 | 3.0 | 3.15 | V |

**ELECTRICAL CHARACTERISTICS (cont.):** Unless otherwise stated, these specifications apply for $T_A$ = 0°C to 70°C for the UCC3750, –40°C to +85°C for the UCC2750, RT = 14k, CT = 470pF, $C_{REF}$ = 0.1µF, FS0 = 0, FS1 = 0, VDD = 5V. $T_A = T_J$.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **Oscillator** | | | | | |
| Accuracy | | 108 | 128 | 148 | kHz |
| Peak Voltage | | | 4.75 | | V |
| Valley Voltage | | | 3 | | V |
| **Charge Pump** | | | | | |
| Switch Pull Up Resistance (VS1, VS2) | | | 15 | 30 | Ω |
| Switch Pull Down Resistance (VS1, VS2) | | | 15 | 30 | Ω |
| Output Voltage (VCP) | VDD = 5V, $I_{VCP}$ = 10mA | | 12 | | V |
| **Output Drivers** | | | | | |
| Pull Up Resistance | | | 9 | 15 | Ω |
| Pull Down Resistance | | | 9 | 15 | Ω |
| Rise Time | CL = 2.7nF | | 50 | 100 | ns |
| Fall Time | CL = 2.7nF | | 50 | 100 | ns |
| **Current Limit** | | | | | |
| AC Limit Threshold Voltage 1 | $\lvert V_{CM} - \text{OUTAC} \rvert$ | | 1.25 | | V |
| | Sine Reference Attenuation | | 25 | | % |
| AC Limit Threshold Voltage 2 | $\lvert V_{CM} - \text{OUTAC} \rvert$ | | 1.5 | | V |
| | Sine Reference Attenuation | | 50 | | % |
| AC Limit Threshold Voltage 3 | $\lvert V_{CM} - \text{OUTAC} \rvert$ | | 1.75 | | V |
| | Sine Reference Attenuation | | 75 | | % |
| DC Limit Threshold Voltage Positive | R5/R6 = 3 | | 0.5 | | V |
| DC Limit Threshold Voltage Negative | R5/R6 = 3 | | –0.5 | | V |
| **Duty Cycle** | | | | | |
| Maximum PWM Duty Cycle | | 48 | 50 | | % |
| Rectifier Duty Cycle | | | 50 | | % |

*Note 1: Guaranteed by measuring the steps of the PWL Sine Wave.*

| State | % VCC | Value for REF = 7.5 | State | % VCC | Value for REF = 7.5 |
|---|---|---|---|---|---|
| 0 | 0.3333 | 2.5 | 5 | 0.4255 | 3.191 |
| 1 | 0.3384 | 2.538 | 6 | 0.4471 | 3.353 |
| 2 | 0.3528 | 2.646 | 7 | 0.4616 | 3.462 |
| 3 | 0.3745 | 2.808 | 8 | 0.4666 | 3.5 |
| 4 | 0.4 | 3 | | | |

## PIN DESCRIPTIONS

**CT:** This pin programs the internal PWM oscillator frequency. Capacitor from CT to GND sets the charge and discharge time of the oscillator.

**ENBL:** Logic input which enables the outputs and the charge pump when high. ENBL should be pulled low to turn the outputs off.

**FS0, FS1:** Frequency select pins for the internal sinewave generator. Table 1 provides the SINREF frequencies as a function of FS0 and FS1 when a 32kHz crystal is used at the crystal inputs (XTAL1, XTAL2). Other proportional frequencies can be obtained with a different crystal. Inputs FS0 and FS1 are TTL compatible.

| FS0 | FS1 | SINREF (Hz) |
|---|---|---|
| 0 | 0 | 20 |
| 1 | 0 | 25 |
| 0 | 1 | 50 |
| 1 | 1 | High Impedance |

**Table 1.**

**GD1:** Output driver that controls the primary side switch in a flyback converter through a gate drive transformer. The output signal on this pin is PWM during positive power transfer modes and zero during negative power transfer modes.

**GD2:** Output driver that controls the p-channel secondary side switch in the flyback converter. The output signal on

## PIN DESCRIPTIONS (cont.)

this pin is PWM during mode 4 (Figure 2) when the reference signal is negative and power is being returned to the input. This pin functions as a synchronous rectifier output during mode 1 with positive reference signal and positive power transfer. This output is logically inverted to provide the correct polarity drive signal for a p-channel switch.

**GD3:** Output driver that controls the n-channel secondary side switch in the flyback converter. The output signal on this pin is PWM during mode 2 (Figure 2) when the reference signal is positive and power is being returned to the input. This pin functions as a synchronous rectifier output during mode 3 with a negative reference signal and positive power transfer.

**GND:** Reference point for the internal reference and all thresholds. Also provides the signal return path for all other pins.

**NEG1:** Inverting input of the buffer amplifier that acts as a summing junction for the DC (battery) offset voltage and sinewave reference.

**NEG2:** Inverting input of the error amplifier where the ringer output voltage and the reference signal with the desired offset are applied with a weighted sum. Feedback compensation is connected between NEG2 and OUT2.

**NEGAC:** Inverting input of the amplifier used to set the AC current limit level.

**NEGDC:** Inverting input of the amplifier used for DC current limiting.

**OUT1:** Output of the buffer amplifier that provides scaling and filtering for the reference signal before feeding it into the error amplifier. This output is also used internally to select the PWM mode for the flyback converter.

**OUT2:** Output of the error amplifier. Used to connect compensation components. This output’s absolute value determines the duty cycle of the PWM pulse. The polarity of this signal also determines the PWM mode.

**OUTAC:** Output node for AC current limit circuit. The AC current limit is activated and the output of SINFLT attenuated when voltage on this pin differs by more than 1.25V from the $V_{CM}$ (= 3V).

**OUTDC:** Output of the DC current limit amplifier. The DC current limit is activated when this pin is above 4.5V or below 1.5V.

**REF:** Internal 7.5V reference. For best results, bypass to GND with a ceramic capacitor(>0.1µF).

**RGOOD:** Logic output that indicates that the error amplifier output is within range ($0 < D < 0.5$). This pin can source upto 0.5mA of current.

**RT:** Resistor from RT to GND helps set the oscillator frequency. RT programs the charge and discharge currents of CT.

**SINFLT:** This signal is the buffered version of SINREF. Under AC limit conditions (such as off-hook detection period), the reference signal amplitude is attenuated. This signal is summed with the DC offset level with appropriate scaling.

**SINREF:** This pin is the output of the sine-wave reference generator. It has a high output impedance (≈ 25kΩ). A 0.01µF capacitor to GND is recommended to provide smoothing of the sinewave. When FS0 and FS1 are both set high, the sine reference generator is disabled allowing this pin to accept an external sinewave input.

**SWRLY:** Logic output that leads the battery offset crossings (by typically 5ms) to allow "zero voltage" relay switching. This pin can typically source 250µA.

**XTAL1:** Crystal connection for external crystal. This pin can be also used to clock the internal sine wave generator when XTAL2 is connected to VDD/2.

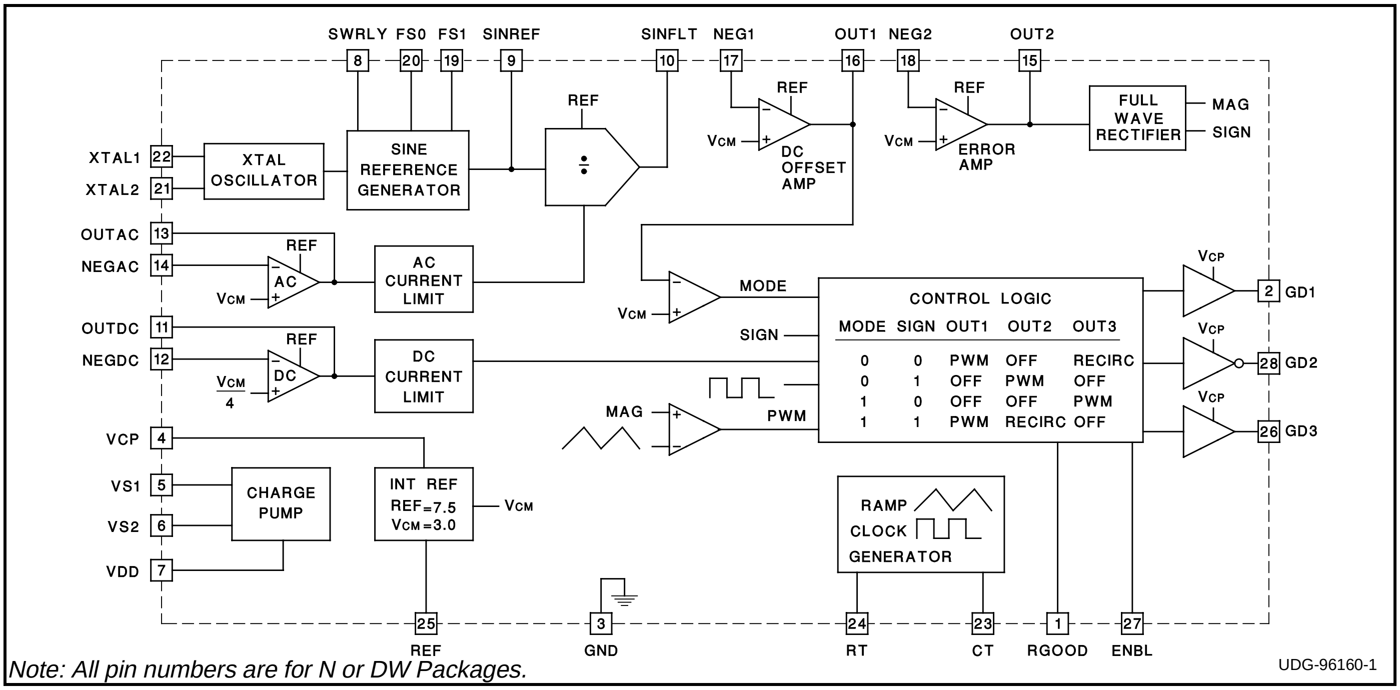
**XTAL2:** Crystal connection for external crystal.

**VCP:** External connection for charge pump storage capacitor. A capacitance ≥ 2.2µF is recommended for low charge pump output ripple. The voltage at this pin is used by the output drivers for gate drive voltages. Alternatively, a regulated gate drive voltage can be connected at this pin while leaving the charge pump circuit at nodes VS1, VS2 disconnected.

**VDD:** External supply input used to bias internal logic functions. Typically a regulated 5V supply is connected between this pin and GND. It also is the input voltage for the voltage tripler circuit to generate the gate drive voltage.

**VS1, VS2:** Voltage switches for the voltage tripler (charge pump circuit). They provide different voltage levels to external capacitors in order to pump up the voltage from VDD to VCP.

## DETAILED BLOCK DIAGRAM

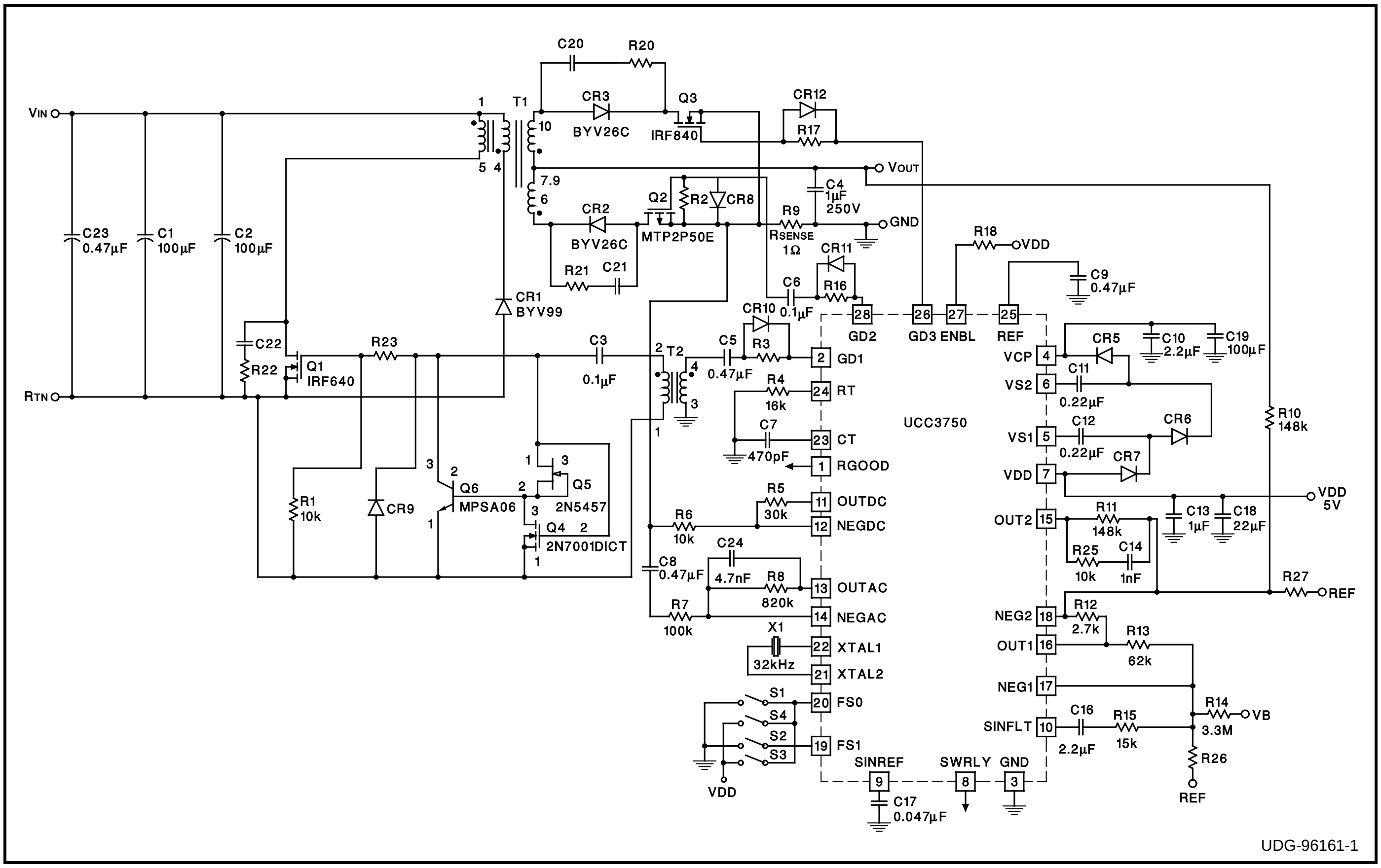


*Note: All pin numbers are for N or DW Packages.*

UDG-96160-1

## APPLICATION INFORMATION

The UCC3750 provides complete control and protection functions for a four quadrant flyback converter used to generate ring signals for telephone circuits. A typical application circuit for a 15 REN ring generator is shown in Figure 1.



UDG-96161-1

Figure 1. Typical Application Circuit

## APPLICATION INFORMATION (cont.)

As shown, the flyback converter takes a DC input (typically 48V) and provides an isolated output with a programmable frequency (and amplitude) AC signal superimposed on a programmable DC offset. The power path consists of a primary side PWM switch Q1, primary return rectifier DR1, a 4-winding transformer T1, output rectifiers DR2 and DR3, synchronous/PWM switches Q2 and Q3, and output filter CF. Resistor $R_{SENSE}$ provides the output current sensing for protection circuits.

Different operating modes of the converter are depicted in Table 2. Figure 2 shows the output voltage and current waveforms for a purely capacitive load and identifies the four operating modes. Figure 3 shows the PWM waveforms for the circuit and Figures 4a - 4d show the equivalent circuits under the operating modes. The addition of Q2, Q3 and primary diode facilitates true four quadrant operation where both the output voltage and power transfer can be bi-directional. Mode 1 is similar to the commonly used DC-DC converter operation where Q1 is modulated with the PWM signal and rectification is provided through the Q2, DR2 path to provide a positive output proportional to the increasing, positive reference voltage. The pulse-width is controlled by the error amplifier output to increase or decrease the output as dictated by the reference. The maximum duty cycle is limited to 50% to prevent DR1 from turning on prior to Q2/DR2.

In mode 2, the reference begins to decrease, necessitating that the power transfer back to the input. For this mode, switch Q3 needs to be modulated while DR1 acts as the rectifier back to the input. The UCC3750 has mode decoding circuitry which automatically directs the PWM signal to Q3 and turns off Q1.

| Mode | Reference Polarity | Power Flow | E.A. Output | Source (PWM) Switch | Rectifier Switch |
|---|---|---|---|---|---|
| 1 | + | + | – | Q1 | Q2 |
| 2 | + | – | + | Q3 | (D1) |
| 3 | – | + | + | Q1 | Q3 |
| 4 | – | – | – | Q2 | (D1) |

**Table 2.**

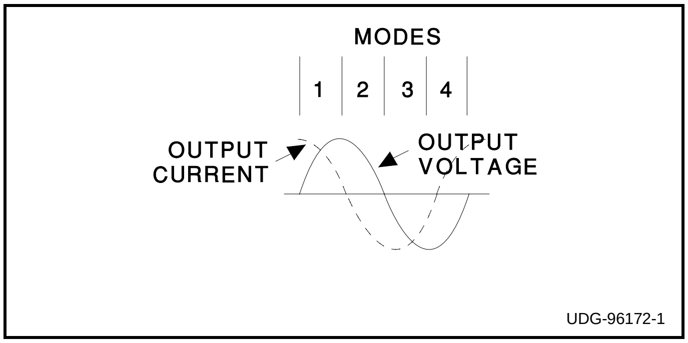


**Figure 2. Operating Modes**

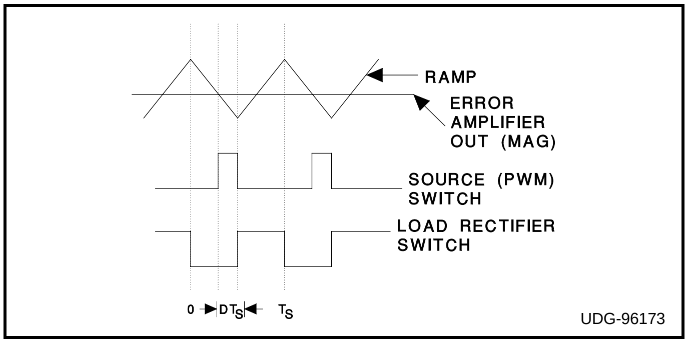


**Figure 3. Circuit Waveforms**

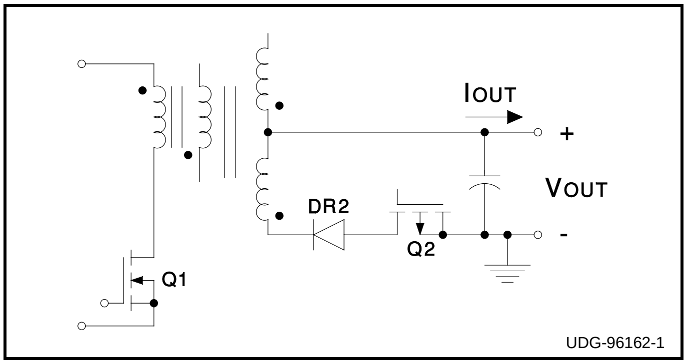


**Figure 4a. Mode 1**
**Forward Power Transfer, Positive Output**

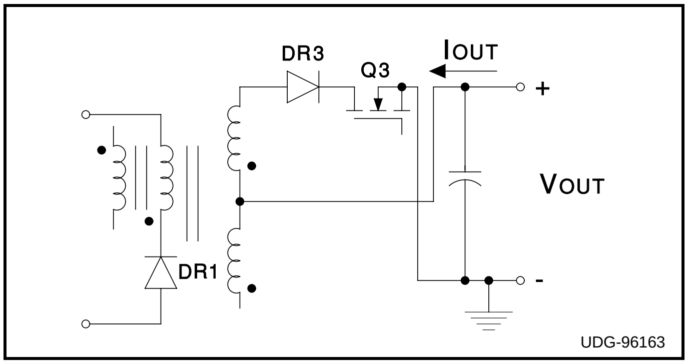


**Figure 4b. Mode 2**
**Reverse Power Transfer, Positive Output**

When the reference signal goes from positive to negative, a transition is made from mode 2 to mode 3. In mode 3, the converter once again acts as a DC-DC flyback converter (with negative output). Similar to mode 1, Q1 is controlled by the PWM output, however, the rectifying path is now through Q3/DR3 as the output polarity is reversed. At the mode boundaries, there could be some distortion which won't affect the THD too much as it is

## APPLICATION INFORMATION (cont.)

near zero crossings. Finally, as the reference signal starts increasing towards zero, the direction of power transfer is again reversed and Q2 is PWMed in mode 4.

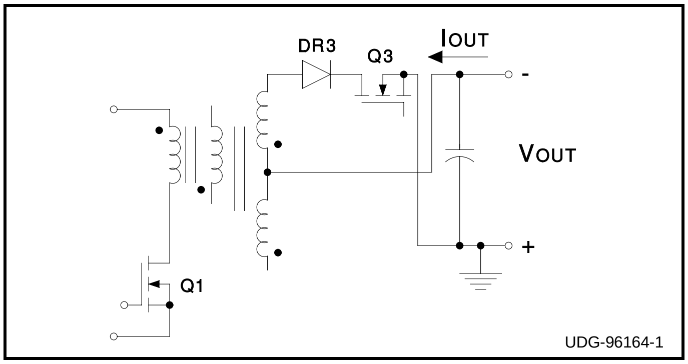


Figure 4c. Mode 3
Forward Power Transfer, Negative Output

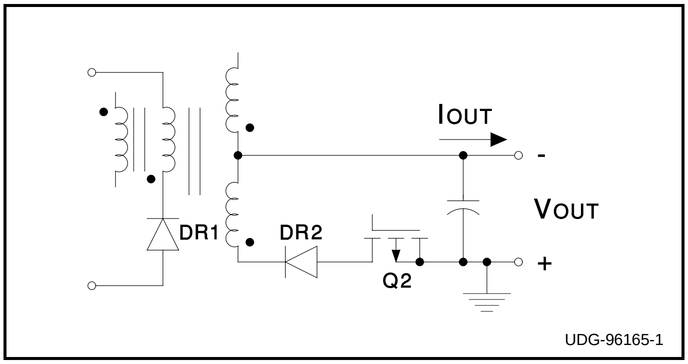


Figure 4d. Mode 4
Reverse Power Transfer, Negative Output

It should be noted that in modes 2 and 3 when the reference is decreasing, the phase of the feedback path is inverted compared to the other two modes. Traditional PWM methods will result in instability due to this characteristic. The UCC3750 separates the error signal magnitude and polarity and determines the correct PWM signal based on a separate mode determination circuit.

## UCC3750 FUNCTIONAL BLOCKS

### Sine Reference Generator

The IC has a versatile low frequency sinewave reference generator with low harmonic distortion and good frequency accuracy. In its intended mode as shown in Figure 5, the reference generator will take an input from a 32kHz crystal (connected between XTAL1 and XTAL2) and generate a sine-wave at 20Hz, 25Hz or 50Hz based on the programming of pins FS0 and FS1 (See Table 2). If the crystal frequency is changed, the output frequencies will be appropriately shifted. C-2 type Quartz crystals (Epson makes available through DigiKey) are recommended for this application. If the frequency accuracy is not a major concern, the more common and less expensive clock crystal (C-type) at 32.768kHz can be used with a minor output frequency offset (20.5Hz instead of 20Hz). Additionally, the XTAL1 input can be clocked at a desired frequency to get a different set of output frequencies at the sine-wave output (with divide ratios of 1600, 1280 and 640). The sine-wave output is centered around an internal reference of 3V. A capacitor from SINREF to GND helps provide smoothing of the sine wave reference. Recommended value is at least 0.01μF and maximum of 0.1μF. When FS0 and FS1 are both 1 (high), the sine reference is disabled and external sine-wave can be fed into the SINREF pin. This signal should have the same DC offset as the internal sine-wave (3V).

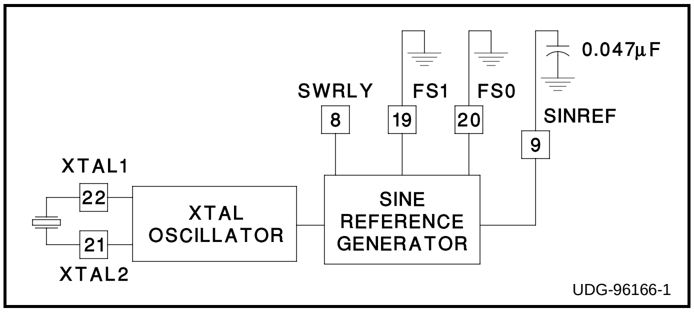


Figure 5. Sine-Wave Generator

### Reference and Error Amplifier

The recommended circuit connections for these circuits are shown in Figure 6. The sine-wave reference is passed through a processing stage that attenuates it in presence of a temporary overload (such as off-hook) condition. The sine-wave is added to a DC offset to create the composite reference signal for the error amplifier. The DC reference can vary over a wide range. For pure AC outputs it is zero, while in many common applications, it is the talk battery voltage (–48V). The UCC3750 accomplishes this task by summing the two signals weighted by resisting R2 and R3. The output of AMP1 also helps determine the mode of the circuit.

Referring to Figure 6, the output of AMP1 is given by :

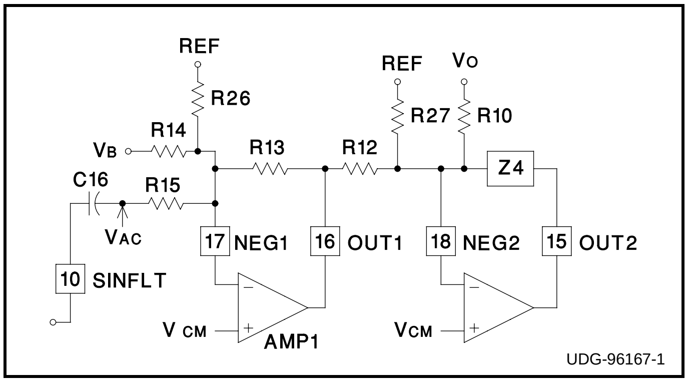


Figure 6. Error Amplifier Setup

## APPLICATION INFORMATION (cont.)

$$V_{OUT1} = \left(1+\frac{R13}{R14}+\frac{R13}{R26}\right)\bullet V_{CM} - \frac{R13}{R26}\bullet REF - \frac{R13}{R14}\bullet V_{B} - \frac{R13}{R15}\bullet V_{AC} \tag{1}$$

In order to nullify the effect of $V_{CM}$ on this value, the ratio of R26 to R14 should be made 1.5. With this ratio, the equation becomes:

$$V_{OUT1} = V_{CM} - \frac{R13}{R14}\bullet V_{B} - \frac{R13}{R15}\bullet V_{AC} \tag{2}$$

VOUT1 is the reference voltage that the second amplifier (AMP2) uses to program the output voltage. Assuming that Z4 is high DC impedance, the output voltage is derived by summing the currents into pin 18. The output is given as:

$$V_{O} = \left(1+\frac{R10}{R27}+\frac{R10}{R12}\right)\bullet V_{CM} - \frac{R10}{R27}\bullet REF - \frac{R10}{R12}\bullet V_{OUT1} \tag{3}$$

Again, if the ratio of R27 to R10 is made 1.5, the effect of $V_{CM}$ is nullified and the output voltage becomes (after substituting for VOUT1):

$$V_{O} = \frac{R10\bullet R13}{R12\bullet R14}\bullet V_{B} + \frac{R10\bullet R13}{R12\bullet R15}\bullet V_{AC} \tag{4}$$

From equation 4, it can be seen that if the output voltage DC value has to track VB directly, the following condition should be forced:

$$R10 \bullet R13 = R12 \bullet R14 \tag{5}$$

However, in some cases, this becomes impractical due to large AC gain required form $V_{AC}$ to $V_{O}$. Only a small part of the gain can be accommodated in the first amplifier stage due to its output voltage limitations. As a result, the required resistance values become very high. This problem is only manifested for high values of VB (e.g. 48V) and can be alleviated by using a fraction of the required DC offset as the VB input and regaining the offset with resistive ratios.

The error amplifier compares the reference signal with the output voltage by way of weighted sum at its inverting input. The error signal is further processed to separate its polarity and magnitude. An absolute value circuit (precision full-wave rectifier) is used to get the magnitude information. The polarity is used along with the reference signal polarity to determine the mode information. The absolute value circuit provides phase inversion when appropriate for modes 2 and 3 to maintain the correct loop gain polarity. While the output of the error amplifier swings around 3V, the full-wave rectifier output (MAG) converts it into a signal above 3V. This signal is compared to the oscillator ramp to generate the PWM output.

### Oscillator and PWM Comparator

The UCC3750 has an internal oscillator capable of high frequency (>250kHz) operation. A resistor on the RT pin programs the current that charges and discharges CT, resulting in a triangular ramp waveform. Figure 7 shows the oscillator hook-up circuit. The ramp peak and valley are 4.75V and 3V respectively. The nominal frequency is given by:

$$f_{OSC} = \frac{1}{1.17 \bullet R_{T} \bullet C_{T}}$$

The ramp waveform and the rectified output of the error amplifier are compared by the PWM comparator to generate the PWM signal. The PWM action is disabled on the positive slope of the ramp signal. Leading edge modulation turns on the PWM signal when the ramp signal falls below MAG on the falling slope and turns it off at the end of the clock cycle. This technique enables synchronized turn-on of the rectifier switches immediately after the PWM pulse is turned off. The triangular nature of the ramp ensures that the maximum duty cycle of the PWM output is 50%, providing inherent current limiting.

### Control Logic and Outputs

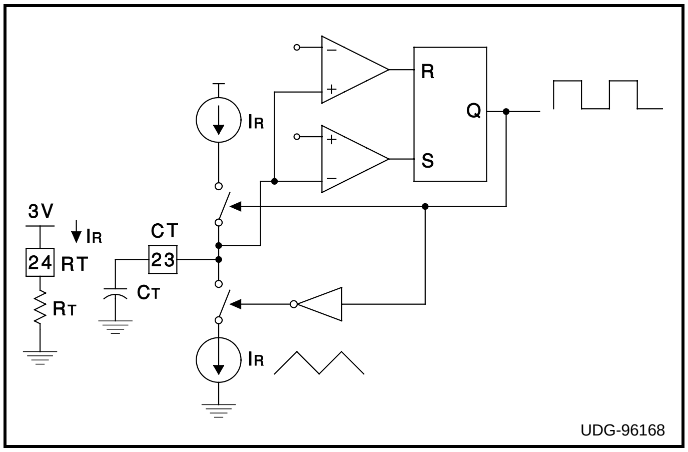


**Figure 7. Oscillator Setup**

The PWM signal is processed through control logic which takes into account the operating mode and output polarity to determine which output to modulate. The logic table for the outputs is given in Table 2. For example, assume that the reference signal is in the first quadrant (positive and increasing). The output will lag the reference by a certain delay and hence the error amp output will be positive, resulting in SIGN = 0. The logic table indicates that GD1 is modulated during this phase allowing power transfer to increase the output voltage to keep up with the reference. Increasing error (MAG) will result in larger duty cycle and

## APPLICATION INFORMATION (cont.)

enable the output to increase and catch up with the reference. If the output becomes higher than the reference (as is likely in the second quadrant when the reference is dropping), the SIGN becomes 1 and GD3 is modulated to decrease the output level by transferring power to the input. At the boundary of the first and second quadrant, there may be some switching back and forth between modes as the reference slope crosses through zero. Some of this switching can be eliminated by judicious selection of error amplifier filtering and compensation components. In the first quadrant, when PWM is applied to Q1, Q2 is turned on in the rectifier mode by the clock signal to allow the flyback transformer flux to reset (and to transfer power to the output). Operation in quadrants 3 and 4 is symmetrical to the first two quadrants with Q2 and Q3 interchanged. Note that the output signal for Q2 is logically inverted to allow for driving the p-channel switch. An n-channel switch can also be used for Q2, but the drive circuit must be transformer isolated and the polarity inverted. The outputs are designed for high peak current drive and low internal impedance. In isolated systems, GD1 must be coupled to Q1 using a gate-drive transformer.

### AC and DC Current Limits

In a typical ring generator application, the load increases significantly when the phone goes off-hook. Under these conditions, it is desired to maintain the output offset level and the sinusoidal shape of the AC component. To limit power consumption the amplitude of the AC signal is allowed to drop. The UCC3750 implements a unique technology to attentuate the ring signal under overload conditions while maintaining the same offset level. The amplifier titled AC tracks the AC part of the current sense signal (as shown in Figure 8) and provides some high frequency filtering. The output of this amplifier (ACOUT) is compared to internal thresholds to determine the attenuation level (if any) for the sinusoidal signal. If this output is within a ± 1.25V window of $V_{CM}$, there is no attenuation of the sine-wave reference and the output is at the externally programmed AC and DC levels. Once the ACOUT goes outside 1.25V of $V_{CM}$, the sine-wave reference is attenuated 25% to reduce the AC level of the output accordingly. When this pin deviates by 1.5V, the output is attenuated 50% and when ACOUT deviates beyond 1.75V, output is attenuated 75%. By programming the gain of the AC amplifier, this circuit can be made to work with any sense resistor value and is independent of DC level current limiting. The decoupling capacitor $C_{AC}$ provides DC decoupling and presents the AC current waveform biased around $V_{CM}$ to the AC amplifier. The attenuation of the output sinewave is accompanied by a shift in the DC level of SINFLT. Depending on the size of the coupling capacitor form SINFLT to AMP1 input, this can result in a transient condition where the AMP1 output is saturated and ring generator output voltage/current are higher than desired. The choice of coupling capacitor should be carefully made to prevent this situation. Alternatively, AC limiting funtion can be disabled (by connecting pins 13 and 14 together) and only the DC limit can be used. The DC current limit function provides protection against short circuit conditions by limiting the maximum current level and shutting off the PWM function when the limit point is reached.

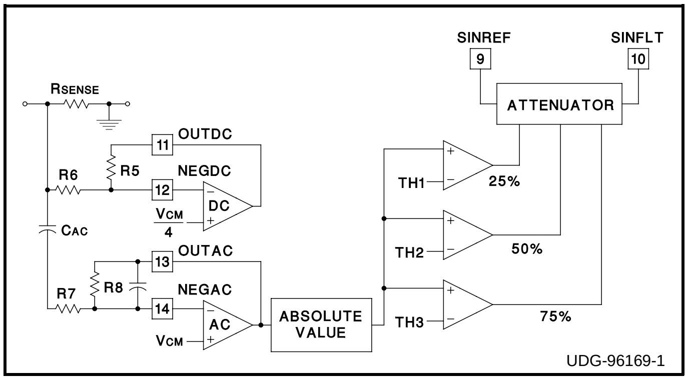


Figure 8. Current Limiting

The DC limit is activated when DC out is below 0.5 $V_{CM}$ or above 1.5 • $V_{CM}$. The DC current limit can be programmed by setting

$$\frac{R5}{R6} = 3.$$

With this ratio, a symmetric DC limit with thresholds of ±0.5V is obtained. For other ratios, the positive and negative voltage thresholds for current sense signal are given by

$$V_{SENSE}(POS) = \frac{V_{CM}}{4} \bullet \left(1 - \frac{R6}{R5}\right)$$

$$V_{SENSE}(NEG) = \frac{V_{CM}}{4} \bullet \left(1 - \frac{5R6}{R5}\right)$$

### Charge Pump and Reference

The UCC3750 is designed to work on the secondary side of an isolated power supply. It requires a 5V power supply with respect to its GND pin to operate. Note that the GND pin of the IC is also the reference point of the ring signal that is generated by the converter. If the converter output is connected in series with any other voltage, it should be ensured that the available supply voltage is referenced to the converter output return. The IC along with its associated charge pump components shown in Figure 9 generates all the other voltages the system re-

## APPLICATION INFORMATION (cont.)

quires. The UCC3750 typically requires about 5mA to operate without any loads on the drive outputs. The charge pump capacitor should be large enough to keep the VCP fairly constant when driving Q1-Q3 in the converter.

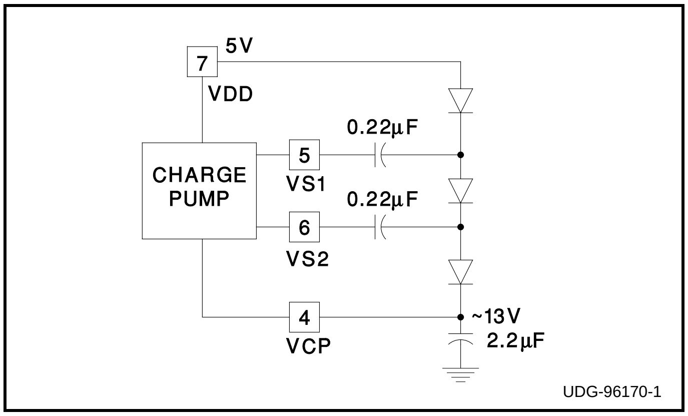


Figure 9. Charge Pump Circuits

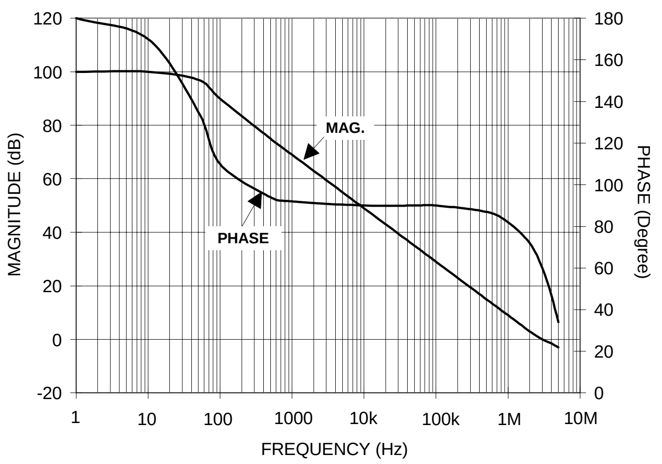


Figure 10. Frequency Response to Error Amplifiers